REMARKS

Claims 1, 3-5, 8, 9, 14, 16-18, have been amended and Claim 23 has been cancelled. No new matter has been added. Applicants respectfully submit that the present set of claims are allowable over the prior art of record.

35 U.S.C. § 102 and 103 Rejections

Claims 1-4, 8-11, and 14-17, and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Austin, U.S. Patent No. 3,163,850 (hereinafter "Austin"); and Claims 5, 7, 12, 13, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Austin, U.S. Patent No. 3,163,850 (hereinafter "Austin").

Austin describes a data processor which is capable of processing a gather instruction and a scatter instruction. The format used for the gather instruction, referred to as a Record Scatter variable ("RSV") instruction, is set forth at column 2, line 67 ("RSV Instruction RSV 0079 3011"). The data processor described in Austin includes dedicated address calculation hardware for processing the RSV instruction. For example, as described at column 5, lines 49-69, when an RSV instruction is encountered during the course of a program routine . . .

> It is fed along Information bus 15 into Program register 24 in the same manner as preceding instruction words. Immediately, the O*p* portion positions sign, 0 and 1, are interpreted by Operation Matrix 33 to initiate the RSV operation.

A musical chairs situation arises as address information is rearranged for the execution of the RSV instruction.
The result of the rearrangement is this:
The single block address is in Address register 29.
The address of the second RDW is in the Address Control register 92.
The first RDW is in the Record Definition register 51.
The RSV execution follows:
Read out data word from address specified by Address register 29 to the Arithmetic register 104. One-up Address register 29. Store data word (Arithmetic register) in working address per Start register 52. Increase working address by variable increment (Variable Increment register 101) and compare with Stop address (Stop register 53).

Thus, Austin describes a processor for processing gather and scatter instructions in an analogous manner to the CRAY-1 vector processor described in the background section of the present application, i.e., using dedicated address calculation registers to hold index vectors and dedicated address calculation hardware.

By contrast, Claim 1 recites a method for performing a gather operation which may be implemented on a general purpose processor and which does not require dedicated hardware. In Claim 1, the gather operation is performed via a plurality of individual instructions. More specifically, to "gather" the data elements stored in memory, an address calculation is performed in which each of a first set of instructions transfers a plurality of indices from a first storage location (e.g., a first general purpose register) where the indices are stored substantially contiguously, to an equal plurality of separate storage locations (e.g., a plurality of additional general purpose registers), wherein each index is assigned its own separate storage location. Then, each of a second set of instructions deposits one or more of the data elements contiguously with other data elements within a

second storage location. Similarly, Claim 14 claims a computer system capable of performing a gather operation using a plurality of instructions rather than dedicated address generation hardware.

In addition, in contrast to Austin, Claim 8 recites a method for performing a scatter operation using a plurality of instructions. Specifically, Claim 8 now recites

> . . . calculating addresses in memory to which a plurality of data elements are to be scattered to form a matrix in memory, wherein each address in memory is identified by one of a plurality of indices and a base address;
>
> executing a plurality of extract instructions, each of said extract instructions extracting one or more of said data elements from a storage location in which said data elements are stored contiguously to an equal plurality of separate storage locations; and
>
> transferring said data elements from said separate storage locations to said calculated addresses in memory.

In sum, Austin does not disclose any mechanism for performing a gather or scatter operation as recited in Claims 1, 8 and 14. Rather, Austin describes using dedicated address calculation registers and address calculation hardware to execute each gather and scatter operation.

Accordingly, Applicants respectfully submit that Claims 1, 8 and 14 and all claims which depend from Claims 1, 8 and 14, including new dependent claims 21-23, are in condition for allowance.

CONCLUSION

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact Thomas Webster at (408) 720-8300.

Respectfully submitted,
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